What is claimed is:

1. A memory device comprising:

a substrate; and

a single transistor formed on the substrate, the transistor having a gate with a nonvolatile memory element.

2. The memory device of claim 1, wherein the nonvolatile memory element is formed between a gate insulating layer and a gate conductive layer, both layers constituting the gate.

3. The memory device of claim 1, wherein the nonvolatile memory element is connected to first and second bit lines separated from each other.

4. The memory device of claim 3, wherein the first and second bit lines pass below the nonvolatile memory element.

5. The memory device of claim 3, wherein the first and second bit lines pass above the nonvolatile memory element.

6. The memory device of claim 1, wherein the nonvolatile memory element includes:

semiconductor quantum dots formed on the gate insulating layer; and

an amorphous material layer covering the plurality of semiconductor quantum dots, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

7. The memory device of claim 6, wherein the semiconductor quantum dots are silicon dots arranged at regular intervals.

8. The memory device of claim 6, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

9. The memory device of claim 2, wherein the nonvolatile memory element includes:

semiconductor quantum dots formed on the gate insulating layer; and

an amorphous material layer covering the plurality of semiconductor quantum dots, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

10. The memory device of claim 9, wherein the semiconductor quantum dots are silicon dots arranged at regular intervals.

11. The memory device of claim 9, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

12. The memory device of claim 3, wherein the nonvolatile memory element includes:

semiconductor quantum dots formed on the gate insulating layer; and

an amorphous material layer covering the plurality of semiconductor quantum dots, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

13. The memory device of claim 12, wherein the semiconductor quantum dots are silicon dots arranged at regular intervals.

14. The memory device of claim 12, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer(SiO_2).

15. The memory device of claim 4, wherein the nonvolatile memory element includes:

semiconductor quantum dots formed on the gate insulating layer; and

an amorphous material layer covering the plurality of semiconductor quantum dots, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

16. The memory device of claim 15, wherein the semiconductor quantum dots are silicon dots arranged at regular intervals.

17. The memory device of claim 15, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

18. The memory device of claim 5, wherein the nonvolatile memory element includes:

semiconductor quantum dots formed on the gate insulating layer; and

an amorphous material layer covering the plurality of semiconductor quantum dots, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

19. The memory device of claim 18, wherein the semiconductor quantum dots are silicon dots arranged at regular intervals.

20. The memory device of claim 18, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

21. The memory device of claim 4, wherein the first and second bit lines are conductive impurity layers formed from the surface of the substrate to a predetermined depth.

22. The memory device of claims 3, wherein a sense amplifier is connected to the first bit line as a current measuring means.

23. The memory device of claim 4, wherein a sense amplifier is connected to the first bit line as a current measuring means.

24. The memory device of claim 5, wherein a sense amplifier is connected to the first bit line as a current measuring means.

25. The memory device of claim 21, wherein a sense amplifier is connected to the first bit line as a current measuring means.

26. A semiconductor memory device comprising:

a substrate;

a transistor formed on the substrate; and

a nonvolatile memory means formed between the transistor and the substrate.

27. The semiconductor memory device of claim 26, wherein the nonvolatile memory means includes an amorphous material layer formed on the substrate and semiconductor quantum dots formed on the amorphous material layer, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a

nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

28. The semiconductor memory device of claim 27, wherein the transistor comprises:

first and second metal layer patterns formed on the amorphous material layer, both being separated from each other;

an insulating layer formed on the amorphous material layer so as to cover the semiconductor quantum dots and the first and second metal layers;

and a word line formed on the insulating layer at a position corresponding to a position where the semiconductor quantum dots are formed.

29. The semiconductor memory device of claim 27, wherein the semiconductor quantum dots are a plurality of spaced silicon dots.

30. The semiconductor memory device of claim 27, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

31. The semiconductor memory device of claim 28, wherein the semiconductor quantum dots are a plurality of spaced silicon dots.

32. The semiconductor memory device of claim 28, further comprising:

an interlayer dielectric layer formed on the insulating layer for covering the word line;

a via hole formed in the interlayer dielectric layer and the insulating layer so that the first metal pattern is exposed; and

a fourth metal layer pattern formed on the interlayer dielectric layer for filling the via hole and passing across the word line.

33. A method for operating a memory device including a single transistor formed on a substrate, wherein the single transistor is a memory transistor having a gate with a nonvolatile memory element, and the nonvolatile memory element is connected to a bit line comprised of first and second bit lines passing across the gate, wherein an addressing voltage and a write voltage are applied to the gate and the bit line, respectively, to write data to the nonvolatile memory element.

34. The method of claim 33, wherein first and second write voltages are applied to the first and second bit lines, respectively, to store data "1" and "0" to the nonvolatile memory element, and the first and second write voltages are the same as or different from each other.

35. The method of claim 33, wherein a second write voltage is applied to the first bit line to store data "1", a first write voltage is applied to the second bit line to store data "0", and the first and second write voltages are the same as or different from each other.

36. The method of claim 33, wherein a first write voltage is applied to the second bit line to store data, and a second write voltage higher than the first write voltage is applied to the second bit line to store different data.

37. The method of claim 33, wherein the written data is read by measuring the conductivity of the nonvolatile memory element.

38. The method of claim 37, wherein an addressing voltage is applied to the gate, and then a current measuring means is connected to the first bit line to measure current between the gate and the first bit line and thus the conductivity of the nonvolatile memory element.

39. The method of claim 38, wherein data "1" or data "0" is read depending on the measured current.

40. A method for operating a memory device including a substrate, a transistor formed on the substrate, the transistor having a gate, a drain connected to a bit line, and a source connected to a source of another transistor, a nonvolatile memory element formed between the gate and the substrate, and a metal line parallel to a word line connected to the transistor, wherein data is written by changing the conductivity of the nonvolatile memory element when the metal line is grounded.

41. The method of claim 40, wherein the nonvolatile memory element is comprised of a material layer for storing carriers, and semiconductor quantum dots formed thereon.

42. The method of claim 41, wherein a write voltage and an addressing voltage are applied to the bit line and the word line, respectively, when the metal line is grounded, to write data by changing the conductivity of the carrier storing material layer.

43. The method of claim 42, wherein data is written by changing the addressing voltage while the write voltage remains constant.

44. The method of claim 42, wherein data is written by changing the write voltage while the addressing voltage remains constant.

45. The method of claim 40, wherein the written data is read by measuring the conductivity of the nonvolatile memory element.

46. The method of claim 45, wherein a read voltage is applied to the bit line, and then a current measuring means is connected to the metal line to measure current between the bit line and the metal line and thus the conductivity of the nonvolatile memory element.

47. The method of claim 46, wherein a different first or second read voltage is applied to the bit line to measure current between the bit line and the metal line and thus read data.

48. The method of claim 45, wherein a read voltage and an addressing voltage are applied to the metal line and the word line, respectively, and then a current measuring means is connected to the bit line to measure current between the metal line and the bit line and thus the conductivity of the nonvolatile memory element.

49. The method of claim 47, wherein data "0" is read when the measured current is large and the data "1" is read when the measured current is small.

50. The method of claim 48, wherein data "0" is read when the measured current is large and the data "1" is read when the measured current is small.

51. A method of manufacturing a memory device comprising:

defining a field region and an active region in a substrate;

forming a field oxide layer on the field region;

forming an insulating layer on the active region;

patterning the insulating layer to form first and second bit lines separated from and parallel to each other on the active region;

forming a memory element for storing data in a nonvolatile state on the insulating layer and the first and second bit lines so that the memory element passes across the first and second bit lines; and

forming a word line on the insulating layer and the memory element.

52. The method of claim 51, wherein the step of forming the memory element further comprises:

forming a plurality of spaced semiconductor quantum layers on the insulating layer and the first and second bit lines; and

forming an amorphous material layer covering the semiconductor quantum dots on the insulating layer.

53. The method of claim 51, wherein the step of forming the memory element comprises:

forming an amorphous material layer on the insulating layer and the first and second bit lines; and

forming spaced semiconductor quantum dots on the amorphous material layer.

54. The method of claim 52, wherein the amorphous material layer is an amorphous dielectric layer.

55. The method of claim 54, wherein the amorphous dielectric layer is formed of an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

56. The method of claim 53, wherein the amorphous material layer is an amorphous dielectric layer.

57. The method of claim 56, wherein the amorphous dielectric layer is formed of an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

58. The method of claim 52, wherein the semiconductor quantum dots are silicon dots for emitting carriers to the amorphous material layer or recapturing the emitted carriers by application of a voltage.

59. The method of claim 53, wherein the semiconductor quantum dots are silicon dots for emitting carriers to the amorphous material layer or recapturing the emitted carriers by application of a voltage.

60. A method of manufacturing a memory device, the method comprising:

forming a nonvolatile amorphous material layer on a substrate; and

forming a transistor on the nonvolatile amorphous material layer so that semiconductor quantum dots for emitting carriers to the amorphous material layer or recapturing the emitted carriers by application of a voltage are formed between the transistor and the amorphous material layer.

61. The method of claim 60, wherein the step of forming the transistor comprises:

forming first and second metal layer patterns on the nonvolatile amorphous material layer;

forming semiconductor quantum dots on the nonvolatile amorphous material layer between the first and second metal layer patterns;

forming a gate insulating layer covering the resultant in which the semiconductor quantum dots are formed on the substrate; and

forming a word line corresponding to the semiconductor quantum dots on the gate insulating layer.

62. The method of claim 60, wherein the nonvolatile amorphous material layer is formed of an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

63. The method of claim 60, wherein the semiconductor quantum dots are silicon dots.

64. The method of claim 61, further comprising:

forming an interlayer dielectric layer covering the word line on the gate insulating layer;

forming a via hole for exposing the first metal layer pattern; and

forming a fourth metal layer pattern for filling the via hole and passing across the word line on the interlayer dielectric layer.